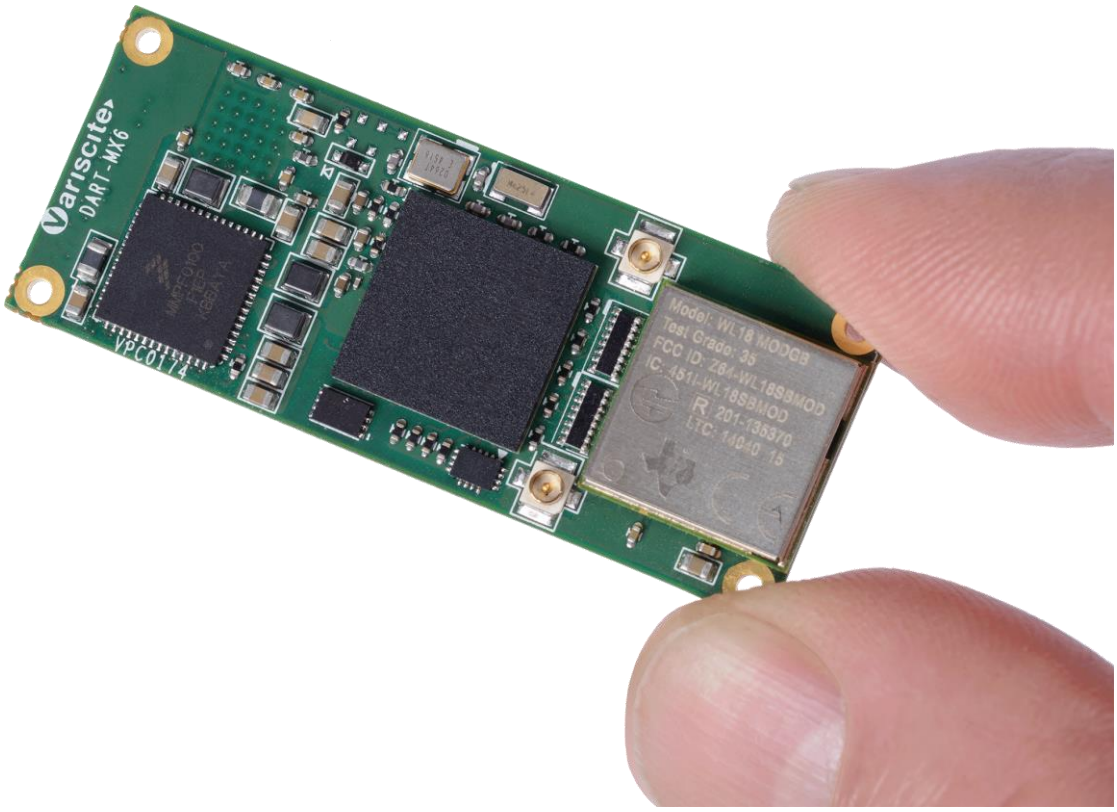
VARISCITE LTD.

DART-MX6 v1.1 Datasheet

Freescale i.MX6™ - based System-on-Module



VARISCITE LTD.

DART-MX6 Datasheet

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Document Revision History

Revision	Date	Notes
1.0	20/04/2015	Initial

1. Overview

1.1. General Information

The DART-MX6 is a high performance System-on-Module. It provides an ideal building block that easily integrates with a wide range of target markets requiring rich multimedia functionality, powerful graphics and video capabilities, as well as high-processing power. Compact, cost effective and with low power consumption, DART-MX6 secures an Intel Atom performance level.

Supporting products:

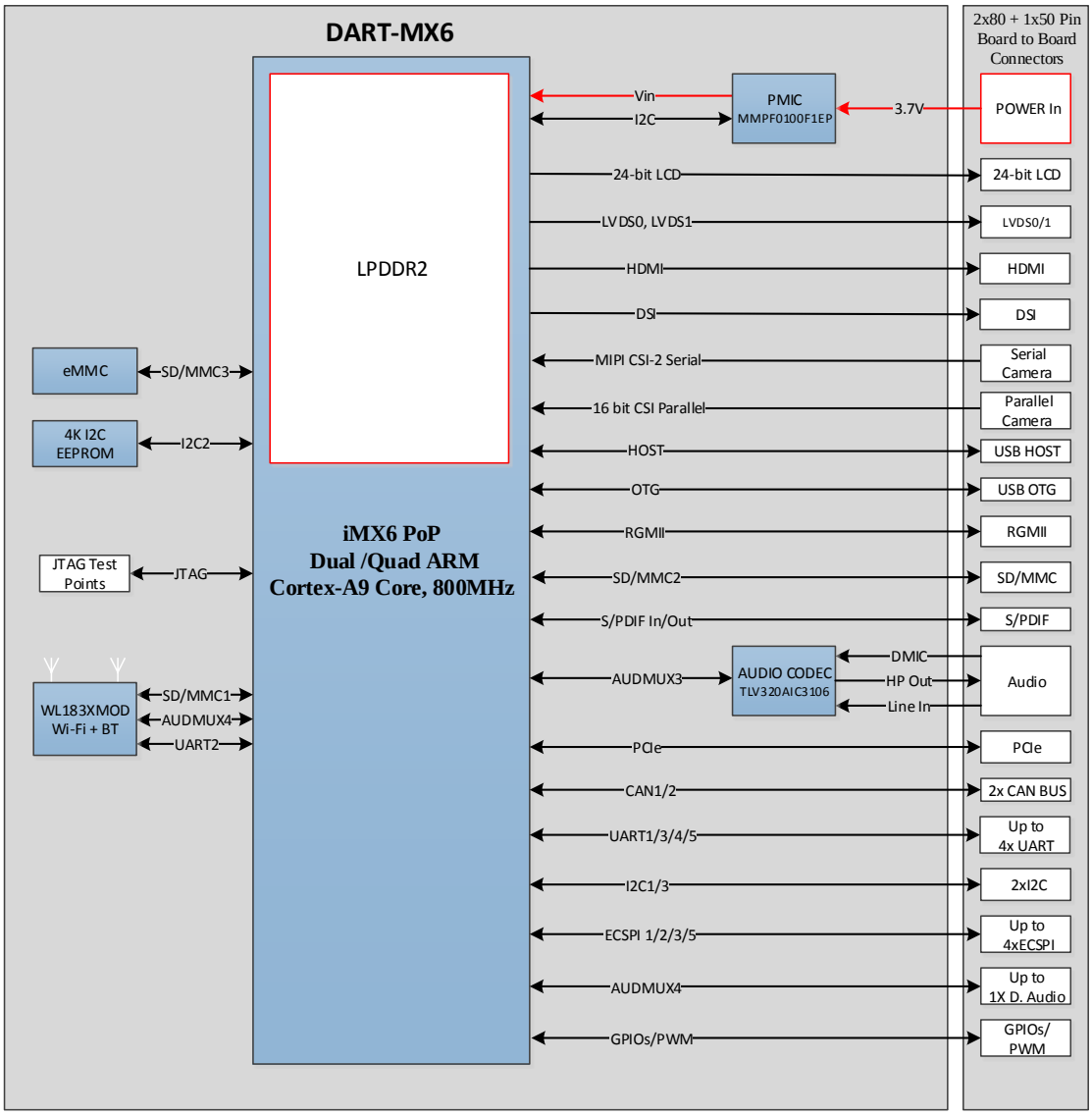
- VAR-DT6CustomBoard– evaluation board
  - ✓ Carrier -Board, compatible with DART-MX6
  - ✓ Schematics
- O.S support
  - ✓ Linux BSP
  - ✓ Windows Embedded Compact 7
  - ✓ Android

Contact Variscite support services for further information: mailto:support@variscite.com.

1.2. Feature Summary

- Freescale i.MX6 series SoC (Dual /Quad ARM® Cortex™-A9 Core, 800Mhz)
- Up to 1GB LPDDR2 RAM
- Up to 64GB eMMC storage
- 24 bit Parallel LCD interface
- 2 x LVDS display interface
- HDMI V1.4 interface
- 1 x MIPI DSI
- Parallel & serial camera interface
- TI WiLink8 2.4/5GHz WLAN (802.11 a/b/g/n) / BT-BLE with optional MIMO
- 1 x USB 2.0 host, 1 x OTG
- 10/100/1000 Mbit/s Ethernet RGMII Interface
- 1 x SD/MMC
- Serial interfaces (SPI , I2C, UART, I2S, SPDIF)
- PCIe
- CAN Bus
- Stereo line-In / headphones out
- Digital microphone
- Single 3.7 V power supply
- 50mm x 20mm, 2x80 + 1x50 pin Board to Board Connectors

1.3. Block Diagram



2. Main Hardware Components

This section summarizes the main hardware building blocks of the DART-MX6

2.1. Freescale i.MX6

2.1.1. Overview

The i.MX6Dual and i.MX6 Quad PoP processors represent Freescale Semiconductor's latest achievement in integrated multimedia applications processors, optimized for lowest power consumption. The processors feature Freescale's advanced implementation of the quad ARM™ Cortex-A9 core, which operates at speeds of up to 800 MHz. They include 2D and 3D graphics processors, 3D 1080p video processing and integrated power management. Each processor provides a 2X32-bit LPDDR2-800 memory interface and a number of other interfaces such as WLAN, Bluetooth™, GPS, hard drive, displays, and camera sensors.

2.1.2. i.MX6 Block Diagram

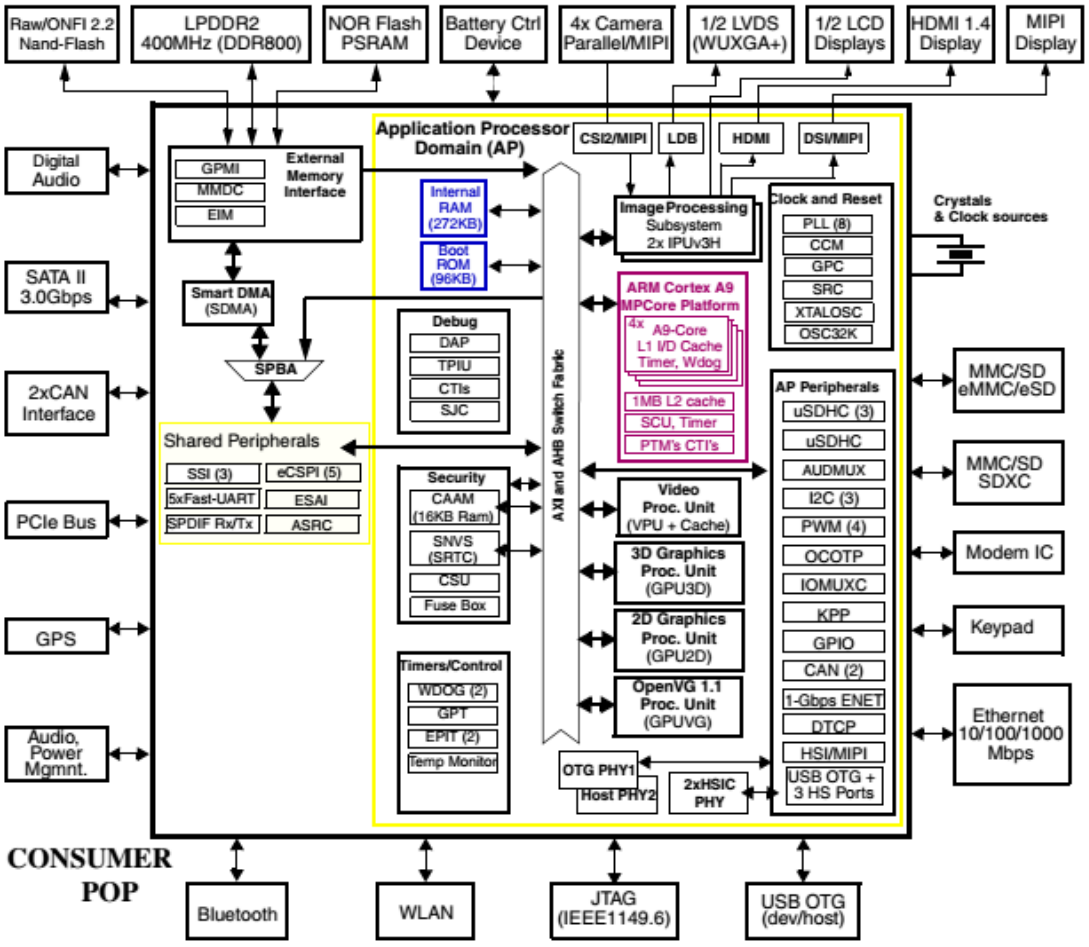


Figure 2. i.MX 6Dual/6Quad Consumer Grade System Block Diagram

2.1.3. CPU Platform

The i.MX6 Dual / Quad Application Processor (AP) is based on the ARM Cortex-A9 MPCore™ Platform, which has the following features:

- ARM Cortex A9 MPCore™ Dual or Quad core CPU configurations (with TrustZone)
- Symmetric CPU configuration where each CPU includes:
  - 32 Kbyte L1 Instruction Cache
  - 32 Kbyte L1 Data Cache
  - Private Timer and Watchdog
  - Cortex-A9 NEON MPE (Media Processing Engine) Co-processor.
- The ARM Cortex A9 MPCore™ complex includes:
- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer
- Snoop Control Unit (SCU)
- 1 Megabyte unified L2 cache shared by all CPU cores (Dual or Quad)
- Two Master AXI (64-bit) bus interfaces output of L2 cache
- NEON MPE coprocessor
  - SIMD Media Processing Architecture
  - NEON register file with 32x64-bit general-purpose registers
  - NEON Integer execute pipeline (ALU, Shift, MAC)
  - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  - NEON load/store and permute pipeline External
  - Supports single and double-precision add, subtract, multiply, divide, multiply and accumulate, and square root operations as described in the ARM VFPv3 architecture.
- Provides conversions between 16-bit, 32-bit and 64-bit floating-point formats and ARM integer word formats.

2.1.4. Memory Interfaces

The memory system consists of the following components:

- Level 1 Cache—32 KB Instruction, 32 KB Data cache per core
- Level 2 Cache—Unified instruction and data (1 MByte)
- On-Chip Memory:
  - Boot ROM, including HAB (96 KB)
  - Internal multimedia / shared, fast access RAM (OCRAM, 256 KB)
  - Secure/non-secure RAM (16 KB)
- External memory interfaces:
  - 2×32-bit, LPDDR2-800 channels supporting DDR interleaving mode
  - 8-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size,
  - BA-NAND, PBA-NAND, LBA-NAND, OneNAND™ and others. BCH ECC up to 40 bit.
- 16-bit NOR Flash. All WEIMv2 pins are muxed on other interfaces.
- 16-bit PSRAM, Cellular RAM

2.1.5. DMA engine

The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features:

- Powered by a 16-bit Instruction-Set micro-RISC engine
- Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels
- 48 events with total flexibility to trigger any combination of channels
- Memory accesses including linear, FIFO, and 2D addressing
- Shared peripherals between ARM and SDMA
- Very fast Context-Switching with 2-level priority based preemptive multi-tasking
- DMA units with auto-flush and prefetch capability
- Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address)
- DMA ports can handle unit-directional and bi-directional flows (copy mode)
- Up to 8-word buffer for configurable burst transfers
- Support of byte-swapping and CRC calculations
- Library of Scripts and API is available

2.1.6. Display Subsystem

The i.MX6Dual/6Quad video graphics subsystem consists of the following dedicated modules:

- Video Processing Unit (VPU): a multi-standard high performance video/image CODEC
- Three Graphics Processing Units (GPUs):
  - 3D GPU: accelerating the generation of 3D graphics (OpenGL/ES) and vector graphics (OpenVG)
  - 2D GPU: acceleration the generation of 2D graphics (BitBLT).
  - OpenVG: acceleration of vector graphics (OpenVG).
- Two (identical) Image Processing Units (IPUs): providing connectivity to cameras and displays, related processing, synchronization and control.
- Display interface bridges: providing optional translation from the digital display interface supported by the IPU to other interfaces:
  - LVDS bridge (LDB): providing up to two LVDS interfaces
  - HDMI transmitter
  - MIPI/DSI transmitter
- MIPI/CSI-2 receiver
- Two (identical) Display Content Integrity Checker (DCIC) are used to authenticate sensitive displayed data.
- A Video Data Order Adapter (VDOA): used to re-order video data from the "tiled" order used by the VPU to the conventional raster-scan order needed by the IPU.

2.1.7. MIPI - Camera Serial Interface Host Controller

The MIPI CSI-2 Host Controller supports the following features:

- Compliant with MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2), Version 1.00 - 29 November 2005

- Optional support for Camera Control Interface (CCI) through the use of DesignWare Core (DW_apb_i2c)
- Interface with MIPI D-PHY following PHY Protocol Interface (PPI), as defined in MIPI Alliance Specification for D-PHY, Version 1.00.00 - 14 May 2009
- Supports up to 4 D-PHY Rx Data Lanes
- Dynamically configurable multi-lane merging
- Long and Short packet decoding
- Timing accurate signaling of Frame and Line synchronization packets; Support for several frame formats such as:
    - General Frame or Digital Interlaced Video with or without accurate sync timing
    - Data type (Packet or Frame level) and Virtual Channel interleaving
- 32-bit Image Data Interface delivering data formatted as recommended in CSI-2 Specification
- Supports all primary and secondary data formats:
    - RGB, YUV and RAW color space definitions
    - From 24-bit down to 6-bit per pixel
    - Generic or user-defined byte-based data types
    - Error detection and correction
    - PHY level
    - Packet level
    - Line level
    - Frame level

2.1.8. 2D and 3D Graphics Processing Unit (GPU)

The GPU2D module has two independent sub-modules: R2D and V2D GPUs. Both GPU were designed to display on a variety of consumer devices. Addressable screen sizes range from small displays featured on cell phones to large 1080p high definition displays.
The GPU2D cores provide powerful graphics at low power consumption, utilizing the smallest silicon footprints. Dynamic power consumption is minimized by extensive use of localized clock gating.
Hardware acceleration is brought to numerous 2D and VG applications including graphical user interfaces (GUI), menu displays, flash animation and gaming.
The GPU3D is a high-performance core that delivers hardware acceleration for 3D graphics display. Addressable screen sizes range from the smallest cell phones to HD 1080p displays. It provides high performance, high quality graphics, low power consumption and the smallest silicon footprint.
GPU3D accelerates numerous 3D graphics applications, including Graphical User Interfaces (GUI), menu displays, flash animation, and gaming. This module supports the following graphics APIs:

- OpenGL ES 2.0
- OpenGL ES 1.1
- OpenVG 1.1
- EGL 1.4
- DirectX 11_9_3
- OpenGL 2.1 and 3.0
- OpenCL 1.1 E

2.1.9. Audio Back End

The AUDMUX provides flexible, programmable routing of the serial interfaces (SSI1 or SSI2) to and from off-chip devices. The AUDMUX routes audio data (and even splices together multiple time-multiplexed audio streams) but does not decode or process audio data itself. The AUDMUX is controlled by the ARM but can route data even when the ARM is in a low-power mode.
The ESAI (Enhanced Serial Audio Interface) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. The ESAI is connected to the IOMUX and to the ESAI_BIFIFO module.
The ESAI_BIFIFO (ESAI Bus Interface and FIFO) is the interface between the ESAI module and the shared peripheral bus. It contains the FIFOs used to buffer data to and from the ESAI, as well as providing the data word alignment and padding necessary to match the 24-bit data bus of the ESAI to the 32-bit data bus of the shared peripheral bus.
The SPDIF (Sony/Philips Digital Interface) audio module is a stereo transceiver that allows the processor to receive and transmit digital audio over it. The SPDIF receiver section includes a frequency measurement block that allows the precise measurement of incoming sampling frequency. A recovered clock is provided by the SPDIF receiver section and may be used to drive both internal and external components in the system. The SPDIF is connected to the shared peripheral bus.
The ASRC (Asynchronous Sample Rate Converter) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. The ASRC supports concurrent sample rate conversions of up to 10 channels of over 120dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates. The ASRC supports up to three sampling rate pairs. The ASRC is connected to the shared peripheral bus.

2.1.10. 10/100/1000 Ethernet Controller

The MAC-NET core, in conjunction with a 10/100/1000 MAC, implements layer 3 network acceleration functions. These functions are designed to accelerate the processing of various common networking protocols, such as IP, TCP, UDP and ICMP, providing wire speed services to client applications. The MAC operation is fully programmable and can be used in NIC (Network Interface Card), bridging, or switching applications. The core implements the remote network monitoring (RMON) counters according to IETF RFC 2819. The core also implements a hardware acceleration block to optimize the performance of network controllers providing IP and TCP, UDP, ICMP protocol services. The acceleration block performs critical functions in hardware, which are typically implemented with large software overhead. The core implements programmable embedded FIFOs that can provide buffering on the receive path for loss-less flow control .Advanced power management features are available with magic packet detection and programmable power-down modes.

2.2. Memory

2.2.1. RAM

The DART-MX6 is available with up to 1 GB of LPDDR2 memory.

2.2.2. Non-volatile Storage Memory

- eMMC: Up to 64GB of storage.

2.3. TLV320AIC3106 Audio

The Texas Instrument's TLV320AIC3106 is a low-power, highly integrated stereo audio codec with stereo headphone amplifier, as well as multiple inputs and outputs programmable in single-ended or fully differential configurations. Extensive register-based power control is included, enabling stereo 48-kHz DAC playback as low as 15mW. The DART-MX6 exposes the following interface of the TLV320AIC3106:

- Headphone
- Line-in
- Digital microphone

2.4. Wi-Fi + BT

The DART-MX6 contains TI's WL183xMOD WiLink, a high performance 2.4/5 GHz IEEE 802.11 a/b/g/n Bluetooth 4.0/BLE radio module with optional Dual Band and MIMO support.
The modules support improved performance over WiFi in bit rates reaching 100Mbps (UDP) and 80Mbps (TCP).
The module realizes the necessary PHY/MAC layers to support WLAN applications in conjunction with a host processor over a SDIO interface.
The module also provides a Bluetooth platform through the HCI transport layer. Both WLAN and Bluetooth share the same antenna port.

- IEEE 802.11 b,g,n or Dual Band 2.4/5GHz 802.11 a/b/g/n with optional MIMO
- Bluetooth 4.0/BLE
- U.FL connectors for external antennas
- Integrated band-pass filter
- Operating Temperature Range:
  Dual Band 2.4/5GHz Modules: -40 to +85
  2.4GHz Modules: -20 to +70

2.5. PMIC

The DART-MX6 features Freescale's PMPF0100 as a Power Management Integrated circuit (PMIC) designed specifically for use with Freescale's i.MX6 series of application processors. The PMPF0100 regulates all power rails required on SoM from a single 3.7 V power supply.
The PMIC is fully programmable via the I2C interface and associated register map. Additional communication is provided by direct logic interfacing including interrupt, watchdog and reset.

3. External Connectors

The DART-MX6 exposes three low profile connectors. Two 80 pin and one 50 pin Board to Board connectors. The recommended mating connectors for Customboard interfacing are:

1. 50 Pin: DF40C-50DS-0.4V(51)
2. 80 Pin: DF40C-80DS-0.4V(51)

Pin#:
Pin number on the SO-DIMM200 connector

Pin Name:
Default DART-MX6 pin name

Type:
Pin type & direction:

- I – In
- O – Out
- DS – Differential Signal
- A – Analog
- Power – Power Pin

Pin Group:
Pin functionality group

i.MX6 Ball:
Ball number

Mode (Tables 3.2 & 3.4):
Pin mux mode option

3.1. DART-MX6 Connector Pin-out

J1					
Pin #	**Pin Name**	**Type**	**Pin Group**	**GPIO**	**i.MX6 Ball**
1	HPLOUT	AO			
2	GND	POWER	Digital GND		
3	HPROUT	AO			
4	LINEIN1_RP	AI			
5	AGND	POWER	Audio GND		
6	LINEIN1_LP	AI			
7	GND	POWER	Digital GND		
8	AGND	POWER	Audio GND		
9	ECSPI1_MISO	IO	Configurable SPI	GPIO4[8]	Y7
10	GND	POWER	Digital GND		
11	ECSPI1_MOSI	IO	Configurable SPI	GPIO4[7]	AB7
12	DMIC_DATA	I	Digital microphone interface		
13	ECSPI1_CLK	IO	Configurable SPI	GPIO4[6]	AB6
14	DMIC_CLK	O	Digital microphone interface		
15	ECSPI1_CS1	IO	Configurable SPI	GPIO4[10]	AD7
16	HDMI_DDCCEC	IO	HDMI		R2
17	GND	POWER	Digital GND		
18	CAN2_TX_OTG_OC	IO	FlexCAN-2	GPIO4[14]	AF1
19	MX6_ONOFF	I	Power On/Off		A13
20	CAN2_RX	I	FlexCAN-2	GPIO4[15]	AC7
21	CAN1_TX	O	FlexCAN-1	GPIO1[7]	AC1
22	HDMI_HPD	I	HDMI		R1
23	CAN1_RX	I	FlexCAN-1	GPIO1[8]	V7
24	GND	POWER	Digital GND		
25	GPIO1[28]	IO	General purpose	GPIO1[28]	AG24
26	VBAT	POWER	3.7 V power supply IN		
27	VBAT	POWER	3.7 V power supply IN		
28	VBAT	POWER	3.7 V power supply IN		
29	VBAT	POWER	3.7 V power supply IN		
30	VBAT	POWER	3.7 V power supply IN		
31	VBAT	POWER	3.7 V power supply IN		
32	VBAT	POWER	3.7 V power supply IN		
33	VBAT	POWER	3.7 V power supply IN		
34	GND	POWER	Digital GND		
35	GND	POWER	Digital GND		
36	UART1_RTS	I	UART1 port	GPIO3[20]	J23

J1					
Pin #	**Pin Name**	**Type**	**Pin Group**	**GPIO**	**i.MX6 Ball**
37	UART3_RTS	I	UART3 port[1], [2]	GPIO2[31]	K27
38	UART1_CTS	O	UART1 port	GPIO3[19]	J29
39	UART3_CTS	O	UART3 port	GPIO3[23]	K24
40	UART1_RXD	I	UART1 port	GPIO5[29]	V1
41	UART3_RXD	I	UART3 port	GPIO3[25]	L28
42	UART1_TXD	O	UART1 port	GPIO5[28]	W3
43	UART3_TXD	O	UART3 port	GPIO3[24]	L29
44	GPIO4_11	IO	General purpose	GPIO4[11]	AF2
45	GPIO1_6	IO	General purpose	GPIO1[6]	AC6
46	GETH_RST	O	Gigabit Ethernet	GPIO1[25]	AG23
47	PWM2	IO	Pulse width modulation 2	GPIO1[1]	AA6
48	POR_B	I	Reset		F13
49	GND	POWER	Digital GND		
50	GND	POWER	Digital GND		

J2					
Pin #	**Pin Name**	**Type**	**Pin Group**	**GPIO**	**i.MX6 Ball**
1	CSI_D0P	DS	Camera serial interface		C1
2	SW4_1V8	POWER	PMIC 1.8V output		
3	CSI_D0M	DS	Camera serial interface		C2
4	CSI_D3M	DS	Camera serial interface		G2
5	CSI_D1M	DS	Camera serial interface		D1
6	CSI_D3P	DS	Camera serial interface		G1
7	CSI_D1P	DS	Camera serial interface		D2
8	CSI_CLK0P	DS	Camera serial interface		E1
9	CSI_D2P	DS	Camera serial interface		F2
10	CSI_CLK0M	DS	Camera serial interface		E2
11	CSI_D2M	DS	Camera serial interface		F1
12	USB_H1_VBUS	I	USB 2.0 5V indication		C11
13	GPIO1_4	IO	General purpose	GPIO1_4	Y6
14	USB_OTG_VBUS	I	OTG 5V indication		G11
15	GND	POWER	Digital GND		
16	GEN_2V5	POWER	PMIC 2.5V output		
17	GND	POWER	Digital GND		
18	USB_H1_OC	I	USB host	GPIO3[30]	N29
19	PCIE_TXP	DS	PCI express interface		B5

J2					
Pin #	**Pin Name**	**Type**	**Pin Group**	**GPIO**	**i.MX6 Ball**
20	GND	POWER	Digital GND		
21	PCIE_TXM	DS	PCI express interface		A5
22	USB_HOST_DN	DS	USB host		B11
23	PCIE_RXP	DS	PCI express interface		A3
24	USB_HOST_DP	DS	USB host		A11
25	PCIE_RXM	DS	PCI express interface		B3
26	GND	POWER	Digital GND		
27	USB_OTG_DN	DS	USB on-the-go		B9
28	HDMI_CLKP	DS	HDMI		L2
29	USB_OTG_DP	DS	USB on-the-go		A9
30	HDMI_CLKM	DS	HDMI		L1
31	GND	POWER	Digital GND		
32	GND	POWER	Digital GND		
33	DSI_D0P	DS	Display serial interface		H1
34	DSI_D1M	DS	Display serial interface		K2
35	DSI_D0M	DS	Display serial interface		H2
36	DSI_D1P	DS	Display serial interface		K1
37	DSI_CLK0P	DS	Display serial interface		J2
38	USB_OTG_ID	I	USB on-the-go	GPIO1[24]	AD22
39	DSI_CLK0M	DS	Display serial interface		J1
40	CLK1_P	DS	PCIE clock		B7
41	ECSPI1_CS0	IO	Configurable SPI	GPIO4[9]	AD3
42	CLK1_N	DS	PCIE clock		A7
43	GND	POWER	Digital GND		
44	HDMI_D0P	DS	HDMI		M2
45	I2C1_SDA	IO	I2C1 interface	GPIO5[26]	W2
46	HDMI_D0M	DS	HDMI		M1
47	I2C1_SCL	IO	I2C1 interface	GPIO5[27]	W1
48	HDMI_D1P	DS	HDMI		N2
49	I2C3_SDA	IO	I2C3 interface	GPIO7[11]	AB2
50	HDMI_D1M	DS	HDMI		N1
51	I2C3_SCL	IO	I2C3 interface	GPIO1[5]	AB3
52	GND	POWER	Digital GND		
53	GND	POWER	Digital GND		
54	HDMI_D2P	DS	HDMI		P2
55	CLKO2	O	Reference clock out	GPIO1[3]	AE1
56	HDMI_D2M	DS	HDMI		P1
57	LVDS0_TX0_N	DS	LVDS0 display bridge		AG2

J2

Pin #	Pin Name	Type	Pin Group	GPIO	i.MX6 Ball
58	LVDS1_TX0_N	DS	LVDS1 display bridge		AJ6
59	LVDS0_TX0_P	DS	LVDS0 display bridge		AG1
60	LVDS1_TX0_P	DS	LVDS1 display bridge		AH6
61	LVDS0_TX1_N	DS	LVDS0 display bridge		AH2
62	LVDS1_TX1_N	DS	LVDS1 display bridge		AH7
63	LVDS0_TX1_P	DS	LVDS0 display bridge		AH1
64	LVDS1_TX1_P	DS	LVDS1 display bridge		AJ7
65	LVDS0_TX2_N	DS	LVDS0 display bridge		AH3
66	LVDS1_TX2_N	DS	LVDS1 display bridge		AJ9
67	LVDS0_TX2_P	DS	LVDS0 display bridge		AJ3
68	LVDS1_TX2_P	DS	LVDS1 display bridge		AH9
69	GND	POWER	Digital GND		
70	GND	POWER	Digital GND		
71	LVDS0_TX3_N	DS	LVDS0 display bridge		AH5
72	LVDS1_TX3_N	DS	LVDS1 display bridge		AJ10
73	LVDS0_TX3_P	DS	LVDS0 display bridge		AJ5
74	LVDS1_TX3_P	DS	LVDS1 display bridge		AH10
75	LVDS0_CLK_N	DS	LVDS0 display bridge		AH4
76	LVDS1_CLK_N	DS	LVDS1 display bridge		AJ8
77	LVDS0_CLK_P	DS	LVDS0 display bridge		AJ4
78	LVDS1_CLK_P	DS	LVDS1 display bridge		AH8
79	GND	POWER	Digital GND		
80	GND	POWER	Digital GND		

J3

Pin #	Pin Name	Type	Pin Group	GPIO	i.MX6 Ball
1	RGMII_TCLK	O	RGMII Interface	GPIO6[19]	C29
2	RGMII_RCLK	I	RGMII Interface	GPIO6[30]	H24
3	RGMII_TCTL	O	RGMII Interface	GPIO6[26]	G28
4	RGMII_RCTL	I	RGMII Interface	GPIO6[24]	F28
5	RGMII_TD0	O	RGMII Interface	GPIO6[20]	C28
6	RGMII_RD0	I	RGMII Interface	GPIO6[25]	G27
7	RGMII_TD1	O	RGMII Interface	GPIO6[21]	E29
8	RGMII_RD1	I	RGMII Interface	GPIO6[27]	F29
9	RGMII_TD2	O	RGMII Interface	GPIO6[22]	G24

J3					
Pin #	**Pin Name**	**Type**	**Pin Group**	**GPIO**	**i.MX6 Ball**
10	RGMII_RD2	I	RGMII Interface	GPIO6[28]	H23
11	RGMII_TD3	O	RGMII Interface	GPIO6[23]	F27
12	RGMII_RD3	I	RGMII Interface	GPIO6[29]	G29
13	GND	POWER	Digital GND		
14	GND	POWER	Digital GND		
15	CSI1_DATA_EN	I	Camera Parallel Interface	GPIO3[10]	Y28
16	SD2_CLK	O	SD/MMC and SDXC	GPIO1[10]	E28
17	CSI1_HSYNCH/BT_CFG2_3	I	Camera Parallel Interface/Boot Select[1]	GPIO3[11]	AE29
18	SD2_DATA0	IO	SD/MMC and SDXC	GPIO1[15]	B29
19	CSI1_VSYNC/BT_CFG2_4	I	Camera Parallel Interface/Boot Select[1]	GPIO3[12]	Y27
20	SD2_CMD	IO	SD/MMC and SDXC	GPIO1[11]	D29
21	CSI1_PIXCLK	I	Camera Parallel Interface	GPIO2[22]	T29
22	SD2_DATA2	IO	SD/MMC and SDXC	GPIO1[13]	B28
23	CSI1_DATA4/BT_CFG1_5	I	Camera Parallel Interface/Boot Select[1]	GPIO3[5]	W28
24	SD2_DATA1	IO	SD/MMC and SDXC	GPIO1[14]	F24
25	CSI1_DATA5	I	Camera Parallel Interface	GPIO3[4]	W27
26	SD2_DATA3	IO	SD/MMC and SDXC	GPIO1[12]	F23
27	GND	POWER	Digital GND		
28	GND	POWER	Digital GND		
29	SPDIFIN	I	SPDIF	GPIO3[21]	K29
30	CSI1_DATA19	I	Camera Parallel Interface	GPIO5[4]	N27
31	SPDIFOUT	O	SPDIFIN	GPIO3[22]	K28
32	CSI1_DATA18	I	Camera Parallel Interface	GPIO6[6]	N28
33	CSI1_DATA8	I	Camera Parallel Interface	GPIO3[1]	V27
34	CSI1_DATA17	I	Camera Parallel Interface	GPIO2[16]	P28
35	CSI1_DATA9	I	Camera Parallel Interface	GPIO3[0]	V28
36	CSI1_DATA16	I	Camera Parallel Interface	GPIO2[17]	P29
37	CSI1_DATA10	I	Camera Parallel Interface	GPIO2[29]	P24
38	CSI1_DATA15	I	Camera Parallel Interface	GPIO2[18]	R29
39	GND	POWER	Digital GND		
40	GND	POWER	Digital GND		
41	CSI1_DATA11	I	Camera Parallel Interface	GPIO2[28]	N23
42	DISP0_VSYNCH	O	LCD Vertical Sync	GPIO4[19]	W24
43	CSI1_DATA12	I	Camera Parallel Interface	GPIO2[21]	N24
44	DISP0_DATA_EN	O	LCD Data Enable	GPIO4[17]	AD28
45	CSI1_DATA13	I	Camera Parallel Interface	GPIO2[20]	M24
46	DISP0_HSYNCH	O	LCD Horizontal Sync	GPIO4[18]	AD29

J3					
Pin #	**Pin Name**	**Type**	**Pin Group**	**GPIO**	**i.MX6 Ball**
47	CSI1_DATA14	I	Camera Parallel Interface	GPIO2[19]	R28
48	ENET_MDC	O	Gigabit Ethernet	GPIO1[31]	AJ21
49	CSI1_DATA6	I	Camera Parallel Interface	GPIO3[3]	AB29
50	ENET_MDIO	IO	Gigabit Ethernet	GPIO1[22]	AJ22
51	CSI1_DATA7	I	Camera Parallel Interface	GPIO3[2]	W29
52	ENET_REF_CLK	I	Gigabit Ethernet	GPIO1[23]	AH21
53	GND	POWER	Digital GND		
54	GND	POWER	Digital GND		
55	DISP0_DAT12	O	LCD Data	GPIO5[6]	AF28
56	DISP0_DAT0	O	LCD Data	GPIO4[21]	AH29
57	DISP0_DAT13	O	LCD Data	GPIO5[7]	AJ25
58	DISP0_DAT1		LCD Data	GPIO4[22]	AD27
59	DISP0_DAT14	IO	LCD Data	GPIO5[8]	AJ28
60	DISP0_DAT2	IO	LCD Data	GPIO4[23]	AB27
61	DISP0_DAT15	IO	LCD Data	GPIO5[9]	AH25
62	DISP0_DAT3	IO	LCD Data	GPIO4[24]	V23
63	DISP0_DAT16	IO	LCD Data	GPIO5[10]	AB24
64	DISP0_DAT4	IO	LCD Data	GPIO4[25]	V24
65	DISP0_DAT17	IO	LCD Data	GPIO5[11]	AH28
66	DISP0_DAT5	IO	LCD Data	GPIO4[26]	AH27
67	GND	POWER	Digital GND		
68	DISP0_CLK	IO	LCD Pixel clock	GPIO4[16]	AF29
69	DISP0_DAT18	IO	LCD Data	GPIO5[12]	AH24
70	DISP0_DAT6	IO	LCD Data	GPIO4[27]	U23
71	DISP0_DAT19	IO	LCD Data	GPIO5[13]	AA24
72	DISP0_DAT7	IO	LCD Data	GPIO4[28]	AE28
73	DISP0_DAT20	IO	LCD Data	GPIO5[14]	AD24
74	DISP0_DAT8	IO	LCD Data	GPIO4[29]	AJ26
75	DISP0_DAT21	IO	LCD Data	GPIO5[15]	AC24
76	DISP0_DAT9	IO	LCD Data	GPIO4[30]	AG28
77	DISP0_DAT22	IO	LCD Data	GPIO5[16]	Y24
78	DISP0_DAT10	IO	LCD Data	GPIO4[31]	AH26
79	DISP0_DAT23	IO	LCD Data	GPIO5[17]	AJ24
80	DISP0_DAT11	IO	LCD Data	GPIO5[5]	AJ27

Note:

[1] Pin is being latched at boot to determine boot sequence.

[2] UART3 RTS- Use with OE# buffer, and enable only after SOM is powered-up. Use reference schematics as example.

3.2. SO-DIMM 200 Pin Mux

The table below summarizes the additional available functionality for each pin in the three board to board connectors.

J1:

PIN	i.MX6 Ball	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
9	Y7	ecspi1. ECSPI1_MISO	enet. ENET_MDIO	audmux. AUD5_TXFS	kpp. KEY_COL1	uart5. UART5_TX_DATA	gpio4. GPIO4_IO08	usdhc1. SD1_VSELECT	
11	AB7	ecspi1. ECSPI1_MOSI	enet. ENET_TX_DATA3	audmux. AUD5_TXD	kpp. KEY_ROW0	uart4. UART4_RX_DATA	gpio4. GPIO4_IO07	dcic2. DCIC2_OUT	
13	AB6	ecspi1. ECSPI1_SCLK	enet. ENET_RX_DATA3	audmux. AUD5_TXC	kpp. KEY_COL0	uart4. UART4_TX_DATA	gpio4. GPIO4_IO06	dcic1. DCIC1_OUT	
15	AD7	ecspi1. ECSPI1_SS1	enet. ENET_RX_DATA2	flexcan1. FLEXCAN1_TX	kpp. KEY_COL2	enet. ENET_MDC	gpio4. GPIO4_IO10	usb. USB_H1_PWR_CTL_WAKE	
18	AF1	flexcan2. FLEXCAN2_TX	ipu1. IPU1_SISG4	usb. USB_OTG_OC	kpp. KEY_COL4	uart5. UART5_RTS_B	gpio4. GPIO4_IO14		
20	AC7	flexcan2. FLEXCAN2_RX	ipu1. IPU1_SISG5	usb. USB_OTG_PWR	kpp. KEY_ROW4	uart5. UART5_CTS_B	gpio4. GPIO4_IO15		
21	AC1	esai. ESAI_TX4_RX1	ecspi5. ECSPI5_RDY	epit1. EPIT1_OUT	flexcan1. FLEXCAN1_TX	uart2. UART2_TX_DATA	gpio1. GPIO1_IO07	spdif. SPDIF_LOCK	usb. USB_OTG_HOST_MODE
23	V7	esai. ESAI_TX5_RX0	xtalosc. XTALOSC_REF_CLK_32K	epit2. EPIT2_OUT	flexcan1. FLEXCAN1_RX	uart2. UART2_RX_DATA	gpio1. GPIO1_IO08	spdif. SPDIF_SR_CLK	usb. USB_OTG_PWR_CTL_WAKE
25	AG24		enet. ENET_TX_EN	esai. ESAI_TX3_RX2			gpio1. GPIO1_IO28		
36	J23	eim. EIM_DATA20	ecspi4. ECSPI4_SS0	ipu1. IPU1_DI0_PIN16	ipu2. IPU2_CSI1_DATA15	uart1. UART1_RTS_B	gpio3. GPIO3_IO20	epit2. EPIT2_OUT	
37	K27	eim. EIM_EB3	ecspi4. ECSPI4_RDY	uart3. UART3_RTS_B	uart1. UART1_RI_B	ipu2. IPU2_CSI1_HSYNC	gpio2. GPIO2_IO31	ipu1. IPU1_DI1_PIN03	src. SRC_BOOT_CFG31
38	J29	eim. EIM_DATA19	ecspi1. ECSPI1_SS1	ipu1. IPU1_DI0_PIN08	ipu2. IPU2_CSI1_DATA16	uart1. UART1_CTS_B	gpio3. GPIO3_IO19	epit1. EPIT1_OUT	
39	K24	eim. EIM_DATA23	ipu1. IPU1_DI0_D0_CS	uart3. UART3_CTS_B	uart1. UART1_DCD_B	ipu2. IPU2_CSI1_DATA_EN	gpio3. GPIO3_IO23	ipu1. IPU1_DI1_PIN02	ipu1. IPU1_DI1_PIN14
40	V1	ipu1. IPU1_CSI0_DATA11	audmux. AUD3_RXFS	ecspi2. ECSPI2_SS0	uart1. UART1_RX_DATA		gpio5. GPIO5_IO29		arm. ARM_TRACE08
41	L28	eim. EIM_DATA25	ecspi4. ECSPI4_SS3	uart3. UART3_RX_DATA	ecspi1. ECSPI1_SS3	ecspi2. ECSPI2_SS3	gpio3. GPIO3_IO25	audmux. AUD5_RXC	uart1. UART1_DSR_B
42	W3	ipu1. IPU1_CSI0_DATA10	audmux. AUD3_RXC	ecspi2. ECSPI2_MISO	uart1. UART1_TX_DATA		gpio5. GPIO5_IO28		arm. ARM_TRACE07
43	L29	eim. EIM_DATA24	ecspi4. ECSPI4_SS2	uart3. UART3_TX_DATA	ecspi1. ECSPI1_SS2	ecspi2. ECSPI2_SS2	gpio3. GPIO3_IO24	audmux. AUD5_RXFS	uart1. UART1_DTR_B
44	AF2	ecspi1. ECSPI1_SS2	enet. ENET_TX_DATA2	flexcan1. FLEXCAN1_RX	kpp. KEY_ROW2	usdhc2. SD2_VSELECT	gpio4. GPIO4_IO11	hdmi. HDMI_TX_CEC_LINE	
45	AC6	esai. ESAI_TX_CLK		i2c3. I2C3_SDA			gpio1.GPIO1_IO06	usdhc2. SD2_LCTL	mlb. MLB_SIG
46	AG23		enet. ENET_RX_EN	Esai ESAI_TX_CLK	spdif. SPDIF_EXT_CLK		gpio1. GPIO1_IO25		
47	AA6	esai. ESAI_RX_CLK	wdog2. WDOG2_B	kpp. KEY_ROW5	usb. USB_OTG_ID	pwm2. PWM2_OUT	gpio1. GPIO1_IO01	usdhc1. SD1_CD_B	

J2:

PIN	i.MX6 Ball	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
13	Y6	esai. ESAI_TX_HF_CLK		kpp. KEY_COL7			gpio1. GPIO1_IO04	usdhc2. SD2_CD_B	
18	N29	eim. EIM_DATA30	ipu1. IPU1_DISP1_DATA21	ipu1. IPU1_DI0_PIN11	ipu1. IPU1_CSI0_DATA03	uart3. UART3_CTS_B	gpio3. GPIO3_IO30	usb. USB_H1_OC	
38	AD22	usb. USB_OTG_ID	enet. ENET_RX_ER	esai. ESAI_RX_HF_CLK	spdif. SPDIF_IN	enet. ENET_1588_EVENT2_OUT	gpio1. GPIO1_IO24		
41	AD3	ecspi1. ECSPI1_SS0	enet. ENET_COL	audmux. AUD5_RXD	kpp. KEY_ROW1	uart5. UART5_RX_DATA	gpio4. GPIO4_IO09	usdhc2. SD2_VSELECT	
45	W2	ipu1. IPU1_CSI0_DATA08	eim. EIM_DATA06	ecspi2. ECSPI2_SCLK	kpp. KEY_COL7	i2c1. I2C1_SDA	gpio5. GPIO5_IO26		arm. ARM_TRACE05
47	W1	ipu1. IPU1_CSI0_DATA09	eim. EIM_DATA07	ecspi2. ECSPI2_MOSI	kpp. KEY_ROW7	i2c1. I2C1_SCL	gpio5. GPIO5_IO27		arm. ARM_TRACE06
49	AB2	esai. ESAI_TX3_RX2	enet. ENET_1588_EVENT2_IN	enet. ENET_REF_CLK	usdhc1. SD1_LCTL	spdif. SPDIF_IN	gpio7. GPIO7_IO11	i2c3. I2C3_SDA	sjc. JTAG_DE_B
51	AB3	Esai ESAI_TX2_RX3		kpp. KEY_ROW7	ccm. CCM_CLKO1		gpio1. GPIO1_IO05	i2c3. I2C3_SCL	arm. ARM_EVENTI
55	AE1	esai. ESAI_RX_HF_CLK		i2c3. I2C3_SCL	xtalosc. XTALOSC_REF_CLK_24M	ccm. CCM_CLKO2	gpio1. GPIO1_IO03	usb. USB_H1_OC	mlb. MLB_CLK

J3:

PIN	i.MX6 Ball	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
1	C29	usb. USB_H2_DATA	enet. RGMII_TXC	spdif. SPDIF_EXT_CLK			gpio6. GPIO6_IO19		xtalosc. XTALOSC_REF_CLK_24M
2	H24	usb. USB_H3_STROBE	enet. RGMII_RXC				gpio6. GPIO6_IO30		
3	G28	usb. USB_H2_STROBE	enet. RGMII_TX_CTL				gpio6. GPIO6_IO26		enet. ENET_REF_CLK
4	F28	usb.USB_H3_DATA	enet. RGMII_RX_CTL				gpio6. GPIO6_IO24		
5	C28	mipi_hsi. HSI_TX_READY	enet. RGMII_TD0				gpio6. GPIO6_IO20		
6	G27	mipi_hsi. HSI_RX_READY	enet. RGMII_RD0				gpio6. GPIO6_IO25		
7	E29	mipi_hsi. HSI_RX_FLAG	enet. RGMII_TD1				gpio6. GPIO6_IO21		
8	F29	mipi_hsi. HSI_TX_FLAG	enet. RGMII_RD1				gpio6. GPIO6_IO27		
9	G24	mipi_hsi. HSI_RX_DATA	enet. RGMII_TD2				gpio6. GPIO6_IO22		
10	H23	mipi_hsi. HSI_TX_DATA	enet. RGMII_RD2				gpio6. GPIO6_IO28		
11	F27	mipi_hsi. HSI_RX_WAKE	enet. RGMII_TD3				gpio6. GPIO6_IO23		
12	G29	mipi_hsi. HSI_TX_WAKE	enet. RGMII_RD3				gpio6. GPIO6_IO29		
15	Y28	eim. EIM_AD10	ipu1. IPU1_DI1_PIN15	ipu2. IPU2_CSI1_DATA_EN			gpio3. GPIO3_IO10		src. SRC_BOOT_CFG10
16	E28	usdhc2. SD2_CLK	ecspi5. ECSPI5_SCLK	kpp. KEY_COL5	audmux. AUD4_RXFS		gpio1. GPIO1_IO10		
17	AE29	eim. EIM_AD11	ipu1. IPU1_DI1_PIN02	ipu2. IPU2_CSI1_HSYNC			gpio3. GPIO3_IO11		src. SRC_BOOT_CFG11
18	B29	usdhc2. SD2_DATA0	ecspi5. ECSPI5_MISO		audmux. AUD4_RXD	kpp. KEY_ROW7	gpio1. GPIO1_IO15	dcic2. DCIC2_OUT	
19	Y27	eim. EIM_AD12	ipu1. IPU1_DI1_PIN03	ipu2. IPU2_CSI1_VSYNC			gpio3. GPIO3_IO12		src. SRC_BOOT_CFG12
20	D29	usdhc2. SD2_CMD	ecspi5. ECSPI5_MOSI	kpp. KEY_ROW5	audmux. AUD4_RXC		gpio1. GPIO1_IO11		
21	T29	eim. EIM_ADDR16	ipu1. IPU1_DI1_DISP_CLK	ipu2. IPU2_CSI1_PIXCLK			gpio2. GPIO2_IO22		src. SRC_BOOT_CFG16
22	B28	usdhc2. SD2_DATA2	ecspi5. ECSPI5_SS1	eim. EIM_CS3	audmux. AUD4_TXD	kpp. KEY_ROW6	gpio1. GPIO1_IO13		
23	W28	eim. EIM_AD05	ipu1. IPU1_DISP1_DATA04	ipu2. IPU2_CSI1_DATA04			gpio3. GPIO3_IO05		src. SRC_BOOT_CFG05
24	F24	usdhc2. SD2_DATA1	ecspi5. ECSPI5_SS0	eim. EIM_CS2	audmux. AUD4_TXFS	kpp. KEY_COL7	gpio1. GPIO1_IO14		
25	W27	eim. EIM_AD04	ipu1. IPU1_DISP1_DATA05	ipu2. IPU2_CSI1_DATA05			gpio3. GPIO3_IO04		src. SRC_BOOT_CFG04
26	F23	usdhc2. SD2_DATA3	ecspi5. ECSPI5_SS3	kpp. KEY_COL6	audmux. AUD4_TXC		gpio1. GPIO1_IO12		
29	K29	eim. EIM_DATA21	ecspi4. ECSPI4_SCLK	ipu1. IPU1_DI0_PIN17	ipu2. IPU2_CSI1_DATA11	usb. USB_OTG_OC	gpio3. GPIO3_IO21	i2c1. I2C1_SCL	spdif. SPDIF_IN
30	N27	eim. EIM_ADDR24	ipu1. IPU1_DISP1_DATA19	ipu2. IPU2_CSI1_DATA19	ipu2. IPU2_SISG2	ipu1. IPU1_SISG2	gpio5. GPIO5_IO04		src. SRC_BOOT_CFG24
31	K28	eim. EIM_DATA22	ecspi4. ECSPI4_MISO	ipu1. IPU1_DI0_PIN01	ipu2. IPU2_CSI1_DATA10	usb. USB_OTG_PWR	gpio3. GPIO3_IO22	spdif. SPDIF_OUT	

PIN	i.MX6 Ball	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
32	N28	eim. EIM_ADDR23	ipu1. IPU1_DISP1_ DATA18	ipu2. IPU2_CSI1_D ATA18	ipu2. IPU2_SISG3	ipu1. IPU1_SISG3	gpio6. GPIO6_IO06		src. SRC_BOOT_CFG23
33	V27	eim. EIM_AD01	ipu1. IPU1_DISP1_ DATA08	ipu2. IPU2_CSI1_D ATA08			gpio3. GPIO3_IO01		src. SRC_BOOT_CFG01
34	P28	eim. EIM_ADDR22	ipu1. IPU1_DISP1_ DATA17	ipu2. IPU2_CSI1_D ATA17			gpio2. GPIO2_IO16		src. SRC_BOOT_CFG22
35	V28	eim. EIM_AD00	ipu1. IPU1_DISP1_ DATA09	ipu2. IPU2_CSI1_D ATA09			gpio3. GPIO3_IO00		src. SRC_BOOT_CFG00
36	P29	eim. EIM_ADDR21	ipu1. IPU1_DISP1_ DATA16	ipu2. IPU2_CSI1_D ATA16			gpio2. GPIO2_IO17		src. SRC_BOOT_CFG21
37	P24	eim. EIM_EB1	ipu1. IPU1_DISP1_ DATA10	ipu2. IPU2_CSI1_D ATA10			gpio2. GPIO2_IO29		src. SRC_BOOT_CFG28
38	R29	eim. EIM_ADDR20	ipu1. IPU1_DISP1_ DATA15	ipu2. IPU2_CSI1_D ATA15			gpio2. GPIO2_IO18		src. SRC_BOOT_CFG20
41	N23	eim. EIM_EB0	ipu1. IPU1_DISP1_ DATA11	ipu2. IPU2_CSI1_D ATA11		ccm. CCM_PMIC _READY	gpio2. GPIO2_IO28		src. SRC_BOOT_CFG27
42	W24	ipu1. IPU1_DI0_PI N03	ipu2. IPU2_DI0_PI N03	audmux. AUD6_TXFS			gpio4. GPIO4_IO19		
43	N24	eim. EIM_ADDR17	ipu1. IPU1_DISP1_ DATA12	ipu2.IPU2_C SI1_DATA12			gpio2. GPIO2_IO21		src. SRC_BOOT_CFG17
44	AD28	ipu1. IPU1_DI0_PI N15	ipu2. IPU2_DI0_PI N15	audmux. AUD6_TXC			gpio4. GPIO4_IO17		
45	M24	eim. EIM_ADDR18	ipu1.IPU1_DI SP1_DATA13	ipu2. IPU2_CSI1_D ATA13			gpio2. GPIO2_IO20		src. SRC_BOOT_CFG18
46	AD29	ipu1. IPU1_DI0_PI N02	ipu2. IPU2_DI0_PI N02	audmux. AUD6_TXD			gpio4. GPIO4_IO18		
47	R28	eim. EIM_ADDR19	ipu1. IPU1_DISP1_ DATA14	ipu2. IPU2_CSI1_D ATA14			gpio2. GPIO2_IO19		src. SRC_BOOT_CFG19
48	AJ21	mlb. MLB_DATA	enet. ENET_MDC	esai. ESAI_TX5_R X0		enet. ENET_1588 _EVENT1_I N	gpio1. GPIO1_IO31		
49	AB29	eim. EIM_AD03	ipu1. IPU1_DISP1_ DATA06	ipu2. IPU2_CSI1_D ATA06			gpio3. GPIO3_IO03		src. SRC_BOOT_CFG03
50	AJ22		enet. ENET_MDIO	Esai .ESAI_RX_CL K		enet. ENET_1588 _EVENT1_O UT	gpio1. GPIO1_IO22	spdif. SPDIF_LOCK	
51	W29	eim. EIM_AD02	ipu1. IPU1_DISP1_ DATA07	ipu2. IPU2_CSI1_D ATA07			gpio3. GPIO3_IO02		src. SRC_BOOT_CFG02
52	AH21		enet. ENET_TX_CL K	esai. ESAI_RX_FS			gpio1. GPIO1_IO23	spdif. SPDIF_SR_CLK	
55	AF28	ipu1. IPU1_DISP0_ DATA12	ipu2. IPU2_DISP0_ DATA12				gpio5. GPIO5_IO06		
56	AH29	ipu1. IPU1_DISP0_ DATA00	ipu2. IPU2_DISP0_ DATA00	ecspi3. ECSPI3_SCLK			gpio4. GPIO4_IO21		
57	AJ25	ipu1. IPU1_DISP0_ DATA13	ipu2. IPU2_DISP0_ DATA13		audmux. AUD5_RXFS		gpio5. GPIO5_IO07		
58	AD27	ipu1. IPU1_DISP0_ DATA01	ipu2. IPU2_DISP0_ DATA01	ecspi3. ECSPI3_MOS I			gpio4. GPIO4_IO22		
59	AJ28	ipu1. IPU1_DISP0_ DATA14	ipu2. IPU2_DISP0_ DATA14		audmux. AUD5_RXC		gpio5. GPIO5_IO08		

PIN	i.MX6 Ball	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
60	AB27	ipu1. IPU1_DISP0_ DATA02	ipu2. IPU2_DISP0_ DATA02	ecspi3. ECSPI3_MIS O			gpio4. GPIO4_IO23		
61	AH25	ipu1. IPU1_DISP0_ DATA15	ipu2. IPU2_DISP0_ DATA15	ecspi1. ECSPI1_SS1	ecspi2. ECSPI2_SS1		gpio5. GPIO5_IO09		
62	V23	ipu1. IPU1_DISP0_ DATA03	ipu2. IPU2_DISP0_ DATA03	ecspi3. ECSPI3_SS0			gpio4. GPIO4_IO24		
63	AB24	ipu1. IPU1_DISP0_ DATA16	ipu2. IPU2_DISP0_ DATA16	ecspi2. ECSPI2_MOS I	audmux. AUD5_TXC	sdma. SDMA_EXT_ EVENT0	gpio5. GPIO5_IO10		
64	V24	ipu1. IPU1_DISP0_ DATA04	ipu2. IPU2_DISP0_ DATA04	ecspi3. ECSPI3_SS1			gpio4. GPIO4_IO25		
65	AH28	ipu1. IPU1_DISP0_ DATA17	ipu2. IPU2_DISP0_ DATA17	ecspi2. ECSPI2_MIS O	audmux. AUD5_TXD	sdma. SDMA_EXT_ EVENT1	gpio5. GPIO5_IO11		
66	AH27	ipu1. IPU1_DISP0_ DATA05	ipu2. IPU2_DISP0_ DATA05	ecspi3. ECSPI3_SS2	audmux. AUD6_RXFS		gpio4. GPIO4_IO26		
68	AF29	ipu1. IPU1_DI0_DI SP_CLK	ipu2. IPU2_DI0_DI SP_CLK						
69	AH24	ipu1. IPU1_DISP0_ DATA18	ipu2. IPU2_DISP0_ DATA18	ecspi2. ECSPI2_SS0	audmux. AUD5_TXFS	audmux. AUD4_RXFS	gpio5. GPIO5_IO12		eim. EIM_CS2
70	U23	ipu1. IPU1_DISP0_ DATA06	ipu2. IPU2_DISP0_ DATA06	ecspi3. ECSPI3_SS3	audmux. AUD6_RXC		gpio4. GPIO4_IO27		
71	AA24	ipu1. IPU1_DISP0_ DATA19	ipu2. IPU2_DISP0_ DATA19	ecspi2. ECSPI2_SCLK	audmux. AUD5_RXD	audmux. AUD4_RXC	gpio5. GPIO5_IO13		eim. EIM_CS3
72	AE28	ipu1. IPU1_DISP0_ DATA07	ipu2. IPU2_DISP0_ DATA07	ecspi3. ECSPI3_RDY			gpio4. GPIO4_IO28		
73	AD24	ipu1. IPU1_DISP0_ DATA20	ipu2. IPU2_DISP0_ DATA20	ecspi1. ECSPI1_SCLK	audmux. AUD4_TXC		gpio5. GPIO5_IO14		
74	AJ26	ipu1. IPU1_DISP0_ DATA08	ipu2. IPU2_DISP0_ DATA08	pwm1. PWM1_OUT	wdog1. WDOG1_B		gpio4. GPIO4_IO29		
75	AC24	ipu1. IPU1_DISP0_ DATA21	ipu2. IPU2_DISP0_ DATA21	ecspi1. ECSPI1_MOS I	audmux. AUD4_TXD		gpio5. GPIO5_IO15		
76	AG28	ipu1. IPU1_DISP0_ DATA09	ipu2. IPU2_DISP0_ DATA09	pwm2. PWM2_OUT	wdog2. WDOG2_B		gpio4. GPIO4_IO30		
77	Y24	ipu1. IPU1_DISP0_ DATA22	ipu2. IPU2_DISP0_ DATA22	ecspi1. ECSPI1_MIS O	audmux. AUD4_TXFS		gpio5. GPIO5_IO16		
78	AH26	ipu1. IPU1_DISP0_ DATA10	ipu2. IPU2_DISP0_ DATA10				gpio4. GPIO4_IO31		
79	AJ24	ipu1. IPU1_DISP0_ DATA23	ipu2. IPU2_DISP0_ DATA23	ecspi1. ECSPI1_SS0	audmux. AUD4_RXD		gpio5. GPIO5_IO17		
80	AJ27	ipu1. IPU1_DISP0_ DATA11	ipu2. IPU2_DISP0_ DATA11				gpio5. GPIO5_IO05		

4. SOM's interfaces

4.1. Display Interfaces

4.1.1. Overview

The DART-MX6 consists of the following display interfaces:

- One parallel Display interface - driven directly by IPU1
- Two LVDS channels, driven by the LDB; pixel clock up to 170 MHz
- One HDMI port (ver. 1.4) - driven by the HDMI transmitter: Pixel clock up to 266 MHz (gated by the IPU capabilities)
- One MIPI/DSI port - driven by the MIPI/DSI transmitter; two data lanes @ 1 GHz
- Each IPU has two display ports. Up to four external ports can be active at any given time (additional asynchronous data flows can be sent though the parallel ports and the MIPI/DSI port).

4.1.2 Parallel Display

The parallel display interface provided by IPU1 consists of 24-bit data bus.

- Supports BT.656 (8-bit) and BT.1120 (16-bit) protocols
- Supports HDTV standards SMPTE274 (1080i/p) and SMPTE296 (720p)

Parallel Display signals:

Signal	Pin #	Type	Description
DISP0_VSYNCH	J3.42	O	LCD Vertical Sync
DISP0_DATA_EN	J3.44	O	LCD Data Enable
DISP0_HSYNCH	J3.46	O	LCD Horizontal Sync
DISP0_CLK	J3.68	O	LCD Pixel Clock
DISP0_DAT0	J3.56	O	LCD Data Line 0
DISP0_DAT1	J3.58	O	LCD Data Line 1
DISP0_DAT2	J3.60	O	LCD Data Line 2
DISP0_DAT3	J3.62	O	LCD Data Line 3
DISP0_DAT4	J3.64	O	LCD Data Line 4
DISP0_DAT5	J3.66	O	LCD Data Line 5
DISP0_DAT6	J3.70	O	LCD Data Line 6
DISP0_DAT7	J3.72	O	LCD Data Line 7
DISP0_DAT8	J3.74	O	LCD Data Line 8
DISP0_DAT9	J3.76	O	LCD Data Line 9
DISP0_DAT10	J3.78	O	LCD Data Line 10
DISP0_DAT11	J3.80	O	LCD Data Line 11
DISP0_DAT12	J3.55	O	LCD Data Line 12
DISP0_DAT13	J3.57	O	LCD Data Line 13
DISP0_DAT14	J3.59	O	LCD Data Line 14
DISP0_DAT15	J3.61	O	LCD Data Line 15
DISP0_DAT16	J3.63	O	LCD Data Line 16

DISP0_DAT17	J3.65	O	LCD Data Line 17
DISP0_DAT18[1]	J3.69	O	LCD Data Line 18
DISP0_DAT19[1]	J3.71	O	LCD Data Line 19
DISP0_DAT20[1]	J3.73	O	LCD Data Line 20
DISP0_DAT21[1]	J3.75	O	LCD Data Line 21
DISP0_DAT22[1]	J3.77	O	LCD Data Line 22
DISP0_DAT23[1]	J3.79	O	LCD Data Line 23

Note:
[1] Pins are shared with on board with Bluetooth Audio connectivity interface.

4.1.3 DSI

DART-MX6 MIPI DSI Host Controller supports up to 2 D-PHY data lanes:

- Bidirectional communication and escape mode support through the data lane
- Programmable display resolutions, from 160 x 120(QQVGA) to 1024 x 768(XVGA)
- Multiple peripheral support capability, configurable virtual channels
- Video mode pixel formats, 16 bpp (5,6,5 RGB), 18 bpp (6,6,6,RGB) packed, 18 bpp (6,6,6,RGB) loosely, 24 bpp (8,8,8,RGB)

DSI signals:

Signal	Pin #	Type	Description
DSI_CLK0M	J2.39	ODS	Negative DSI clock differential
DSI_CLK0P	J2.37	ODS	Positive DSI clock differential
DSI_D0M	J2.35	ODS	Negative DSI data 0 differential
DSI_D0P	J2.33	ODS	Positive DSI data 0 differential
DSI_D1M	J2.34	ODS	Negative DSI data 1 differential
DSI_D1P	J2.36	ODS	Positive DSI data 1 differential

4.1.4 HDMI

The HDMI module provides an HDMI standard interface port to an HDMI 1.4 compliant display

HDMI Signals:

Signal	Pin #	Type	Description
HDMI_CLKM	J2.30	ODS	Negative HDMI clock differential
HDMI_CLKP	J2.28	ODS	Positive HDMI clock differential
HDMI_D0M	J2.46	ODS	Negative HDMI data 0 differential
HDMI_D0P	J2.44	ODS	Positive HDMI data 0 differential
HDMI_D1M	J2.50	ODS	Negative HDMI data 1 differential
HDMI_D1P	J2.48	ODS	Positive HDMI data 1 differential
HDMI_D2M	J2.56	ODS	Negative HDMI data 2 differential
HDMI_D2P	J2.54	ODS	Positive HDMI data 2 differential
HDMI_DDCCEC	J1.16	IO	One wire bidirectional CEC
HDMI_HPD	J1.22	I	Hot plug detect

4.1.5 LVDS Interface

LVDS Display Bridge (LDB) will be used to connect the IPU (Image Processing Unit) to the External LVDS display interface.
There are 2 LVDS channels. These outputs are used to communicate RGB data and controls to external LCD displays.
The LVDS ports may be used as follows:

- Single channel output
- Dual channel output (one input source, two channel outputs for two displays)
- Split channel output (one input source, split to two channels on output)
- Separate two channel output (two input sources from IPU)

LVDS0 Signals:

Signal	Pin #	Type	Description
LVDS0_TX0_N	J2.57	ODS	Negative data 0 differential
LVDS0_TX0_P	J2.59	ODS	Positive data 0 differential
LVDS0_TX1_N	J2.61	ODS	Negative data 1 differential
LVDS0_TX1_P	J2.63	ODS	Positive data 1 differential
LVDS0_TX2_N	J2.65	ODS	Negative data 2 differential
LVDS0_TX2_P	J2.67	ODS	Positive data 2 differential
LVDS0_TX3_N	J2.71	ODS	Negative data 3 differential
LVDS0_TX3_P	J2.73	ODS	Positive data 3 differential
LVDS0_CLK_N	J2.75	ODS	Negative clock differential
LVDS0_CLK_P	J2.77	ODS	Positive clock differential

LVDS1 Signals:

Signal	Pin #	Type	Description
LVDS1_TX0_N	J2.58	ODS	Negative data 0 differential
LVDS1_TX0_P	J2.60	ODS	Positive data 0 differential
LVDS1_TX1_N	J2.62	ODS	Negative data 1 differential
LVDS1_TX1_P	J2.64	ODS	Positive data 1 differential
LVDS1_TX2_N	J2.66	ODS	Negative data 2 differential
LVDS1_TX2_P	J2.68	ODS	Positive data 2 differential
LVDS1_TX3_N	J2.72	ODS	Negative data 3 differential
LVDS1_TX3_P	J2.74	ODS	Positive data 3 differential
LVDS1_CLK_N	J2.76	ODS	Negative clock differential
LVDS1_CLK_P	J2.78	ODS	Positive clock differential

4.2. Camera Interfaces

4.2.1. MIPI CSI-2

The CSI-2 Host Controller is a digital core that implements all protocol functions defined in the MIPI CSI-2 specification, providing an interface between the system and the MIPI D-PHY, allowing communication with an MIPI CSI-2 compliant camera sensor.

The MIPI CSI-2 host controller supports the following features:

- Compliance with MIPI Alliance standard for camera serial interface 2 (CSI-2), version 1.00 29th November, 2005
- Optional support for Camera Control Interface (CCI) through the use of DesignWare Core (DW_apb_i2c)
- Interface with MIPI D-PHY following PHY Protocol Interface (PPI), as defined in MIPI Alliance Specification for D-PHY, version 1.00.00 14th May, 2009
- Supports up to 4 D-PHY Rx data lanes
- Dynamically configurable multi-lane merging
- Long and short packet decoding
- Timing accurate signaling of frame and line synchronization packets
- Support for several frame formats such as:
  - General frame or digital interlaced video with or without accurate sync timing
  - Data type (packet or frame level) and virtual channel interleaving
- 32-bit image data interface delivering data formatted as recommended in CSI-2 specification
- Supports all primary and secondary data formats:
  - RGB, YUV and RAW color space definitions
  - From 24-bit down to 6-bit per pixel
  - Generic or user-defined byte-based data types
  - Error detection and correction:
    - PHY level
    - Packet level
    - Line level
    - Frame level

MIPI CSI-2 signals:

Signal	Pin #	Type	Description
CSI_CLK0M	J2.10	IDS	Negative CSI-2 clock differential
CSI_CLK0P	J2.8	IDS	Positive CSI-2 clock differential
CSI_D0M	J2.3	IDS	Negative CSI-2 data 0 differential
CSI_D0P	J2.1	IDS	Positive CSI-2 data 0 differential
CSI_D1M	J2.5	IDS	Negative CSI-2 data 1 differential
CSI_D1P	J2.7	IDS	Positive CSI-2 data 1 differential
CSI_D2M	J2.11	IDS	Negative CSI-2 data 2 differential
CSI_D2P	J2.9	IDS	Positive CSI-2 data 2 differential
CSI_D3M	J2.4	IDS	Negative CSI-2 data 3 differential
CSI_D3P	J2.6	IDS	Positive CSI-2 data 3 differential

4.2.2. Parallel CSIx

Based on i.MX6 IPU, the DART-MX6 supports a camera port controlled by IPU2 CSI1 sub-block, providing a connection to image sensors and related devices.

CSI1 Signals:

Signal	Pin #	Type	Description
CSI1_DATA4/ BT_CFG1_5 [1]	J3.23	I	Camera data line
CSI1_DATA5	J3.25	I	Camera data line
CSI1_DATA6	J3.49	I	Camera data line
CSI1_DATA7	J3.51	I	Camera data line
CSI1_DATA8	J3.33	I	Camera data line
CSI1_DATA9	J3.35	I	Camera data line
CSI1_DATA10	J3.37	I	Camera data line
CSI1_DATA11	J3.41	I	Camera data line
CSI1_DATA12	J3.43	I	Camera data line
CSI1_DATA13	J3.45	I	Camera data line
CSI1_DATA14	J3.47	I	Camera data line
CSI1_DATA15	J3.38	I	Camera data line
CSI1_DATA16	J3.36	I	Camera data line
CSI1_DATA17	J3.34	I	Camera data line
CSI1_DATA18	J3.32	I	Camera data line
CSI1_DATA19	J3.30	I	Camera data line
CSI1_DATA_EN	J3.15	I	Camera data enable
CSI1_HSYNCH/ BT_CFG2_3 [1]	J3.17	I	Camera horizontal sync
CSI1_PIXCLK	J3.21	I	Camera pixel clock
CSI1_VSYNC/ BT_CFG2_4 [1]	J3.19	I	Camera vertical sync

Note:

[1] Pin is being latched at boot to determine boot sequence. Please refer to boot options section.

4.3. Gigabit Ethernet

Gigabit Ethernet Features:

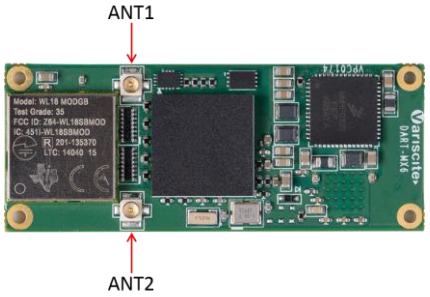
The Ethernet Media Access Controller (MAC) is designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. An external Gigabit PHY MIcrel's KSZ9031RNXCA and magnetics is used on carrier board to complete the interface to the media. The i.MX6 processor also consists of HW assist for IEEE1588 standard. See the IEEE1588 section for more details.

Signal	Pin #	Type	Description
RGMII_RCLK	J3.2	I	RGMII Receive Clock
RGMII_RCTL	J3.4	I	RGMII Receive Control
RGMII_RD0	J3.6	I	RGMII Receive Data Bit 0
RGMII_RD1	J3.8	I	RGMII Receive Data Bit 1
RGMII_RD2	J3.10	I	RGMII Receive Data Bit 2
RGMII_RD3	J3.12	I	RGMII Receive Data Bit 3
RGMII_TCLK	J3.1	O	RGMII Transmit Clock
RGMII_TCTL	J3.3	O	RGMII Transmit Control
RGMII_TD0	J3.5	O	RGMII Transmit Data Bit 0
RGMII_TD1	J3.7	O	RGMII Transmit Data Bit 1
RGMII_TD2	J3.9	O	RGMII Transmit Data Bit 2
RGMII_TD3	J3.11	O	RGMII Transmit Data Bit 3

4.4. Wi-Fi & Bluetooth

The DART-MX6 contains TI's WL183xMOD WiLink, a high performance 2.4/5 GHz IEEE 802.11 a/b/g/n Bluetooth 4.0/BLE radio module with optional Dual Band and MIMO support.
The modules support improved performance over WiFi in bit rates reaching 100Mbps (UDP) and 80Mbps (TCP).
The module realizes the necessary PHY/MAC layers to support WLAN applications in conjunction with a host processor over a SDIO interface.
The module also provides a Bluetooth platform through the HCI transport layer. Both WLAN and Bluetooth share the same antenna port.

- IEEE 802.11 b,g,n or Dual Band 2.4/5GHz 802.11 a/b/g/n with optional MIMO
- Bluetooth 4.0/BLE
- U.FL connectors for external antennas
- Integrated band-pass filter
- Operating Temperature Range:
  Dual Band 2.4/5GHz Modules: -40 to +85
  2.4GHz Modules: -20 to +70



4.5. USB Host 2.0

The USB controller block provides high performance USB functionality that conforms to the USB 2.0 specification.

USB Host1 Signals:

Signal	Pin #	Type	Description
USB_HOST_DP	J2.24	IODS	Positive USB host data
USB_HOST_DN	J2.22	IODS	Negative USB host data
USB_H1_VBUS	J2.12	I	USB 2.0 VBUS indicator (5V)
USB_H1_OC	J2.18	I	USB host over current indicator , Active low 3.3v digital

4.6. USB 2.0 OTG

USB 2.0 On-the-go Features:

High-speed OTG core

- HS/FS/LS UTMI compliant interface
- High speed, full speed and low speed operation in host mode (with UTMI transceiver)
- High speed, and full speed operation in peripheral mode (with UTMI transceiver)
- Hardware support for OTG signaling, session request protocol, and host negotiation protocol
- Up to 8 bidirectional endpoints
- Integrated HS USB PHY

OTG Signals:

Signal	Pin #	Type	Description
USB_OTG_DN	J2.27	IODS	Negative USB OTG data
USB_OTG_DP	J2.29	IODS	Positive USB OTG data
USB_OTG_VBUS	J2.14	I	USB 2.0 OTG VBUS indicator (5V)
USB_OTG_ID	J2.38	I	USB OTG host/client ID Low : Host mode Float: Client mode

4.7. MMC/SD/SDIO

MX6 MMC interface features:

- Fully compliant with MMC command/response sets and physical layer as defined in the Multimedia Card System specification v4.2/4.3/4.4, including high-capacity (size > 2 GB) cards HC MMC.
- Fully compliant with SD command/response sets and physical layer as defined in the SD Memory Card specifications v3.0, including high-capacity SDHC cards up to 32 GB
- Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card specification, Part E1 v1.10
- Fully compliant with SD Card specification, Part A2, SD Host Controller Standard specification v2.00
- 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max)

- 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max). However, the SoC level integration and I/O muxing logic restrict functionality to the following:

SDMMC2 Signals:

Signal	Pin #	Type	Description
SD2_CLK	J3.16	O	Clock for MMC/SD/SDIO card
SD2_CMD	J3.20	O	CMD line connect to card
SD2_DATA0	J3.18	IO	DAT0 line in all modes (also used to detect busy state)
SD2_DATA1	J3.24	IO	DAT1 line-in
SD2_DATA2	J3.22	IO	DAT2 line
SD2_DATA3	J3.26	IO	DAT3 line-in

4.8. Audio

The DART-MX6 features three audio interfaces:

- TLV320AIC3106 Audio codec interfaces
    1. Analog outputs / inputs:
        - stereo line-in
        - Stereo HP out
    2. Digital microphone input
- SSI Digital audio interface
- S/PDIF in/out

Analog audio signals are featured by the on-SOM TLV320AIC3106 audio codec. Refer to the data sheet for detailed electrical characteristics of the relevant interfaces http://www.ti.com/product/tlv320aic3106.

Analog Signals:

Signal	Pin #	Type	Description
HPLOUT	J1.1	AO	Headphones out - left
HPROUT	J1.3	AO	Headphones out - right
LINEIN1_RP	J1.4	AI	Line-in - Right
LINEIN1_LP	J1.6	AI	Line-in - Left

Digital AUDMUX:

Key features of the block include:

- Full 6-wire SSI interfaces for asynchronous receive and transmit
- Configurable 4-wire (synchronous) or 6-wire (asynchronous) peripheral interfaces
- Independent Tx/Rx frame sync and clock direction selection for host or peripheral
- Each host interface's capability to connect to any other host or peripheral interface in a point-to-point or point-to-multipoint (network mode)
- Transmit and receive data switching to support external network mode

AUDMUX4 Signals:

Signal	Pin #	Type	Description
AUDMUX4_TXD[1]	J3.75	IO	Transmit data from pin
AUDMUX4_RXD[1]	J3.79	IO	Receive data at pin
AUDMUX4_TXC[1]	J3.73	IO	Transmit clock input/output at pin
AUDMUX4_RXC[1]	J3.71	IO	Receive clock input/output at pin
AUDMUX4_TXFS[1]	J3.77	IO	Transmit frame sync input/output at pin
AUDMUX4_RXFS[1]	J3.69	IO	Receive frame sync input/output at pin

Note:
[1] AUDMUX4 Signals are shared with the on-som Bluetooth Audio Interface and LCD lines. Refer to Parallel Display chapter for more details

S/PDIF (Sony Phillips Digital Interface) In/Out:

S/PDIF is a standard audio file transfer format, developed jointly by the Sony and Phillips corporations.

SPIDF Signals:

Signal	Pin #	Type	Description
SPDIFIN	J3.29, J2.38 (MUXED), J2.49(MUXED)	I	In
SPDIFOUT	J3.31	O	Out
Spdif.lock	J1.21(MUXED), J3.50(MUXED)	O	Lock signal
Spdif.srclk	J1.23(MUXED), J3.52(MUXED),	O	SR Lock signal
SPDIF_EXT_CLK	J1.46 (MUXED), J3.1 (MUXED)	I	External clock signal

4.9. UART Interfaces

By default four UART interfaces are supported, refer to Table 3.2 for further configurations the UART interface.

UART Features:

Each of the UART modules support the following serial data transmit/receive protocols and configurations:

- 7or 8-bit data words, one or two stop bits, programmable parity (even, odd or none)
- Programmable baud rates up to 4 MHz This is a higher max baud rate relative to the 1.875 MHz, which is stated by the TIA/EIA-232-F standard and the i.MX31 UART modules.
- 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud
- IrDA 1.0 support (up to SIR speed of 115200 bps)

UART1 Signals:

Signal	Pin #	Type	Description
UART1_TXD	J1.42	O	UART transmit
UART1_RXD	J1.40	I	UART receive
UART1_RTS	J1.36	I	UART HW flow control RTS
UART1_CTS	J1.38	O	UART HW flow control CTS

Note: UART1 is used as default boot debug port.

UART3 Signals:

Signal	Pin #	Type	Description
UART3_TXD	J1.43	O	UART transmit
UART3_RXD	J1.41	I	UART receive
UART3_RTS[1]	J1.37	I	UART HW flow control RTS
UART3_CTS	J1.39, J2.18(MUXED)	O	UART HW flow control CTS

Note:
[1] UART3 RTS pin is being latched at boot to determine boot sequence. Use with OE# buffer, and enable only after SOM is powered-up. Use reference schematics as example.

UART4 Signals:

Signal	Pin #	Type	Description
UART4_TXD	J1.13(MUXED)	O	UART transmit
UART4_RXD	J1.11(MUXED)	I	UART receive

UART5 Signals:

Signal	Pin #	Type	Description
UART5_TXD	J1.9(MUXED)	O	UART transmit
UART5_RXD	J2.41(MUXED)	I	UART receive
UART5_RTS	J1.18(MUXED)	I	UART HW flow control RTS
UART5_CTS	J1.20(MUXED)	O	UART HW flow control CTS

4.10. Flexible Controller Area Network (FLEXCAN)

The CAN protocol was primarily, but not exclusively, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: Real-time processing, reliable operation in the Electromagnetic Interference (EMI) environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, version 2.0 B, which supports both standard and extended message frames.

CAN1 Signals:

Signal	Pin #	Type	Description
CAN1_TX	J1.21, J1.15(MUXED)	O	CAN BUS transmit
CAN1_RX	J1.23, J1.44(MUXED)	I	CAN BUS receive

CAN2 Signals:

Signal	Pin #	Type	Description
CAN2_TX	J1.18	O	CAN BUS transmit
CAN2_RX	J1.20	I	CAN BUS receive

Signal Descriptions
CAN Rx: The receive pin from the CAN bus transceiver. Dominant state is represented by logic level '0'. Recessive state is represented by logic level '1'.
CAN Tx: The transmit pin to the CAN bus transceiver. Dominant state is represented by logic level '0'. Recessive state is represented by logic level '1'.

4.11. SPI

The Enhanced Configurable Serial Peripheral Interface (ECSPI) is a full-duplex, synchronous 4-wire serial communication block. The ECSPI contains a 64 x 32 receive buffer (RXFIFO) and a 64 x 32 transmit buffer (TXFIFO). With data FIFOs, the ECSPI allows rapid data communication with fewer software interruptions.

4.11.1. eCSPI Key Features:

- Full-duplex synchronous serial interface
- Master/slave configurable
- Four chip select (SS) signals to support multiple peripherals
- Transfer continuation function allows unlimited length data transfers
- 32-bit wide by 64-entry FIFO for both transmitting and receiving data
- 32-bit wide by 16-entry FIFO for HT message data
- Polarity and phase of the chip select (SS) and SPI clock (SCLK) are configurable
- Direct Memory Access (DMA) support
- Max operation frequency up to the reference clock frequency

ECSPI1 Signals:

Signal	Pin #	Type	Description
ECSPI1_CLK	J1.16, J3.73(MUXED)	IO	SPI1 clock
ECSPI1_MOSI	J1.11, J3.75(MUXED)	IO	SPI1 MOSI signal
ECSPI1_MISO	J1.9, J3.77(MUXED)	IO	SPI1 SOMI signal
ECSPI1_CS0	J2.41, J3.79(MUXED)	IO	SPI1 chip select 0 signal
ECSPI1_CS1	J1.15, J1.38(MUXED), J3.61(MUXED)	IO	SPI1 chip select 1 signal
ECSPI1_CS2	J1.43(MUXED), J1.44(MUXED)	IO	SPI1 chip select 2 signal
ECSPI1_CS3	J1.41 (MUXED)	IO	SPI1 chip select 3 signal

ECSPI2 Signals:

Signal	Pin #	Type	Description
ECSPI2_CLK	J3.69(MUXED), J3.71(MUXED)	IO	SPI2 clock
ECSPI2_MOSI	J2.47(MUXED), J3.63(MUXED)	IO	SPI2 MOSI signal
ECSPI2_MISO	J1.42(MUXED), J3.65(MUXED)	IO	SPI2 SOMI signal

ECSPI2_CS0	J1.40(MUXED), J3.69(MUXED)	IO	SPI2 Chip select 0 signal
ECSPI2_CS1	J3.61 (MUXED)	IO	SPI2 Chip select 1 signal
ECSPI2_CS2	J1.43(MUXED)	IO	SPI2 Chip select 2 signal
ECSPI2_CS3	J1.41(MUXED)	IO	SPI2 Chip select 3 signal

ECSPI3 Signals:

Signal	Pin #	Type	Description
ECSPI3_CLK	J3.56(MUXED)	IO	SPI3 clock
ECSPI3_MOSI	J3.58(MUXED)	IO	SPI3 MOSI signal
ECSPI3_MISO	J3.60(MUXED)	IO	SPI3 SOMI signal
ECSPI3_CS0	J3.62(MUXED)	IO	SPI3 Chip select 0 signal
ECSPI3_CS1	J3.64(MUXED)	IO	SPI3 Chip select 1 signal
ECSPI3_CS2	J3.66(MUXED)	IO	SPI3 Chip select 2 signal
ECSPI3_CS3	J3.70(MUXED)	IO	SPI3 Chip select 3 signal
ECSPI3_RDY	J3.72(MUXED)	I	SPI3 ready signal

ECSPI5 Signals:

Signal	Pin #	Type	Description
ECSPI5_CLK	J3.16(MUXED)	IO	SPI5 clock
ECSPI5_MOSI	J3.20(MUXED)	IO	SPI5 MOSI signal
ECSPI5_MISO	J3.18(MUXED)	IO	SPI5 SOMI signal
ECSPI5_CS0	J3.24(MUXED)	IO	SPI5 Chip select 0 signal
ECSPI5_CS1	J3.22(MUXED)	IO	SPI5 Chip select 1 signal
ECSPI5_CS3	J3.26(MUXED)	IO	SPI5 Chip select 3 signal
ECSPI5_RDY	J1.21(MUXED)	I	SPI5 ready signal

4.12. PCIe

DART-MX6 PCI Express functionality has the following parts:

PCI Express includes the following cores:

- PCI Express Dual Mode (DM) core
- PCI Express Root Complex (RC) core
- PCI Express Endpoint (EP) core

PCI Express 2.0 PHY:

- PCIe 2.0 PHY is a complete mixed-signal semiconductor intellectual property (IP) solution, designed for single-chip integration into computer applications
- The PCIe 2.0 PHY supports both the 5 Gbps data rate of the PCI Express Gen 2.0 specifications as well as being backwards compatible to the 2.5Gb/s Gen 1.1 specification

PCIE Signals:

Signal	Pin #	Type	Description
PCIE_TXP	J2.19	DS	Positive PCI TX differential
PCIE_TXM	J2.21	DS	Negative PCI TX differential
PCIE_RXP	J2.23	DS	Positive PCI RX differential
PCIE_RXM	J2.25	DS	Negative PCI RX differential
CLK1_P	J2.40	DS	Positive PCI clock differential
CLK1_N	J2.42	DS	Negative PCI clock differential

4.13. I²C

I2C-1, 2, 3 Interface connectivity peripherals provide serial interface for external devices. Data rates of up to 400 kbps are supported.

I2C1 Signals:

Signal	Pin #	Type	Description
I2C1_SCL	J2.47, J3.29(MUXED)	IO	I2C1 I²C clock, open drain
I2C1_SDA	J2.45	IO	I2C1 I²C data, open drain

I2C3 Signals:

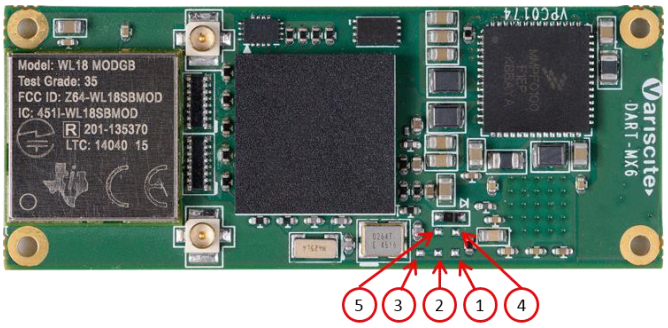
Signal	Pin #	Type	Description
I2C3_SCL	J2.51, J2.55(MUXED)	IO	I2C3 I²C clock, open drain
I2C3_SDA	J2.49, J1.45(MUXED)	IO	I2C3 I²C data, open drain

4.14. JTAG

The System JTAG Controller (SJC) provides debug and test control with maximum security. The test access port (TAP) is designed to support features compatible with the IEEE standard 1149.1 v2001 (JTAG). Support IEEE P1149.6 extensions to the JTAG standard are for AC testing of selected IO signals. The JTAG Interface is exported through Test Points.

JTAG signals 40-pin FFC Connector:

Signal	TP #	Type	Description
JTAG_TDI	5	I	JTAG data-in
JTAG_NTRST	4	I	JTAG reset
JTAG_TMS	3	I	JTAG test mode select
JTAG_TCK	1	O	JTAG test clock
JTAG_TDO	2	O	JTAG data-out



4.15. General Purpose IOs

Most of the SoM's IO pins can be used as GPIOs.
Please refer to Chapter 3, for complete SoM connectors signal list and GPIO multiplexing.

4.16. General System Control

4.16.1. Boot Options

Below you can find the MX6 boot options

8	7	6	5	4	3	2	1
BT_CFG1_7	BT_CFG1_6	BT_CFG1_5	BT_CFG1_4	BT_CFG2_6	BT_CFG2_5	BT_CFG2_4	BT_CFG2_3
1XXX = NANDF Boot							
011X = MMC/eMMC Boot				X0 = 1-bit X1 = 4-bit 10 = 8-bit		01 = SD2 Boot 10 = SD3 Boot 11 = SD4 Boot	
010X = SD/eSD Boot				X0 = 1-bit X1 = 4-bit		01 = SD2 Boot 10 = SD3 Boot 11 = SD4 Boot	
0011 = Serial ROM (SPINOR) Boot							
0010 = SATA Boot							

The boot-select pin configures the boot sequence of the DART-MX6:
BOOT_CFG = 01X001XX

Pin Name	Pin Number	MX6 BOOT_CFG	Internally pulled
CSI1_DATA4/BT_CFG1_5	J3.23	BT_CFG1_5	Pulled-up 10K
CSI1_VSYNC/BT_CFG2_4	J3.19	BT_CFG2_4	Pulled-up 10K
CSI1_HSYNCH/BT_CFG2_3	J3.17	BT_CFG2_3	Pulled-down 10K

Use cases:
BOOT_CFG = 01100110 => SD3 boot, on-SOM eMMC Boot, 4 bit bus
BOOT_CFG = 01000101 => SD2 boot, on carrier SD-Card, 4 bit bus

4.16.2. Reset

'0' logic will reset DART-MX6

4.16.3. Reference Clock Out

DART-MX6 output clock (CLKO2) is controlled by the i.MX6 CCM module. Please refer to the i.MX6 user manual regarding the configuration option for this clock.

4.16.4. General System Control Signals

Signal	Pin #	Type	Description
CLKO	J2.55	O	Clock out
CSI1_DATA4/BT_CFG1_5	J3.23	I	Refer to section 4.16.1
CSI1_VSYNC/BT_CFG2_4	J3.19	I	Refer to section 4.16.1
CSI1_HSYNCH/BT_CFG2_3	J3.17	I	Refer to section 4.16.1
POR_B	J1.48	I	Hardware reset
MX6_ONOFF	J1.19	I	Power on/off

4.17. Power

4.17.1. Power Supply

Signal	Pin #	Type	Description
VBAT	J1.26, J1.27 J1.28, J1.29 J1.30, J1.31 J1.32, J1.33	Power In	DART-MX6 Single DC-IN Supply voltage. Voltage range: 3.7 +/- 5%

4.17.2. Ground

Signal	Pin #	Type	Description
GND	J1.2, J1.7, J1.10, J1.17, J1.24, J1.34, J1.35, J1.49, J1.50, J2.15, J2.17, J2.20, J2.26, J2.31, J2.32, J2.43, J2.52, J2.53, J2.69, J2.70, J2.79, J2.80, J3.13, J3.14, J3.27,J3.28, J3.39, J3.40, J3.53, J3.54, J3.67	Power	Digital ground
AGND	J1.5, J1.8	Power	Analog GND

5. Absolute Maximum Characteristics

Power Supply	Min	Max	Unit
Main Power Supply, DC-IN	-0.3	4.8	V

6. Operational Characteristics

6.1. Power supplies

	Min	Typical	Max	Unit
Main Power Supply, DC-IN	-5%	3.7	+5%	V

6.2. Power Consumption

CPU usage:

Task	SOM VBAT current draw in ma @3.7v
Idle (~10% CPU) @ 400mhz	220mA
FHD Video playback	365mA
100% CPU Dhrystone test – Dual core	400mA
100% CPU Dhrystone test – Quad core	650mA

Additional peripherals:

Task	SOM VBAT current draw in ma @3.7v
WLAN transmission	~320mA
Gbit Ethernet	~410mA

7. DC Electrical Characteristics

Parameter	Min	Typical	Max	Unit
Digital 3.3V				
V_{IH}	0.7x VIN_3V3		VIN_3V3	V
V_{IL}	0		0.3x VIN_3V3	V
V_{OH}	VIN_3V3- 0.15			V
V_{OL}			0.15	V

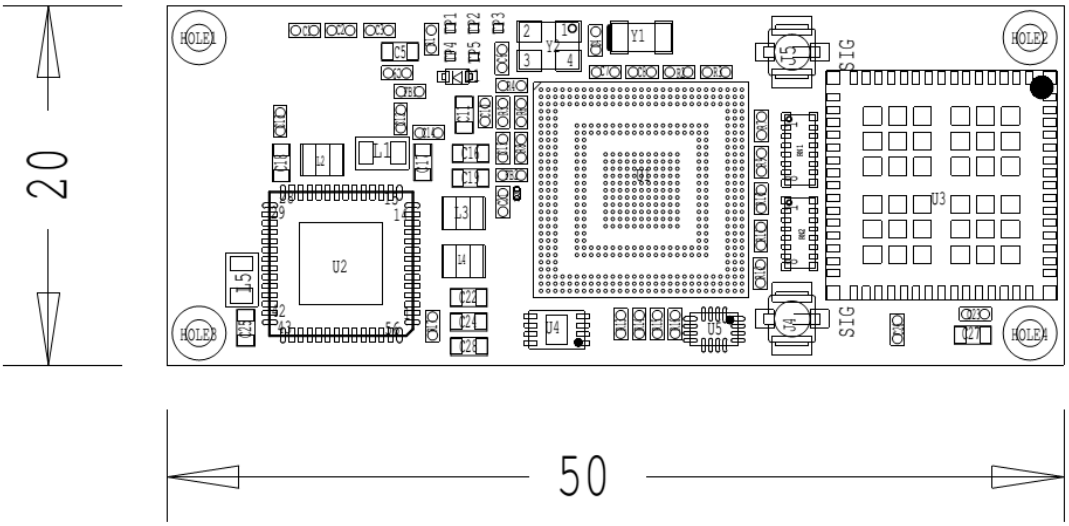
8. Environmental Specifications

	Min	Max
Commercial Operating Temperature Range	0 ^{0}C	+70 ^{0}C
Extended Operating Temperature Range	-20 ^{0}C	+70 ^{0}C
Industrial Operating Temperature Range	-40 ^{0}C	+85 ^{0}C
Referring MIL-HDBK-217F-2 Parts Count Reliability Prediction Method Model: 50Deg Celsius, Class B-1, GM 50Deg Celsius, Class B-1, GB	 121 Khrs > 1400 Khrs >	
Shock Resistance	50G/20 ms	
Vibration	20G/0 - 600 Hz	

Note: Extended and Industrial Temperature is only based on the operating temperature grade of the SoM components. Customer should consider specific thermal design for the final product based upon the specific environmental and operational conditions.

9. Mechanical Drawings

Top View [mm]



CAD files are available for download at http://www.variscite.com/

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